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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,792	06/08/2001	Hector Sanchez	SC11391TC	6921

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/877,792	SANCHEZ ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 August 2005 has been entered.

Claims 1-6 and 9-40 are pending in this application. Claims 1-6 and 9-40 have been rejected.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-6, 9-40 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 37 recite a limitation of "providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature" (emphasis added) which renders the claim indefinite. It is unclear from the language of the claim whether the recited features are

performed as components of the method. It is unclear how the recited functions contribute to the claimed method.

Claim 1 recites a method that is functionally equivalent to:

A method for making an integrated circuit, comprising:

Providing a first circuit design;

Changing the first circuit design to obtain a second circuit design; and

Making an integrated circuit comprising the second circuit design.

None of the other recited steps contribute to the stated purpose of the preamble. The steps of "providing a circuit simulator", "providing an equation", "applying the circuit simulator to the first circuit design", "replacing the unknown constants", and "performing a first set of timing analyses" are unrelated to the result of the method, specifically the "integrated circuit comprising the second circuit design". The language of claim 1 fails to particularly point out and distinctly claim the invention by reciting several steps that do not contribute to the method.

Similarly, Claim 37 recites a method that is functionally equivalent to:

A method for obtaining a performance model, comprising:

Providing a path comprising a first design block, a second design block, and an interconnect coupling the first design block to the second design block;

Changing the design of at least one of the interconnect, the first design block, and the second design block to obtain a revised path; and

Making an integrated circuit comprising the revised path.

The language of claim 37 fails to particularly point out and distinctly claim the invention by reciting several steps that do not contribute to the method.

Claim 2 recites additional steps of claim 1, apparently to be performed after the completion of the method of claim 1, however claim 1 has achieved the stated purpose of the preamble. In that circumstance, the steps of claim 2 would fail to contribute to the method, which has been fulfilled by claim 1, and these steps would be, at best, optional. Claim 2 is vague and indefinite for at least the ambiguity regarding the sequence of steps and whether the steps of claim 2 contribute to the method.

Claim 3 recites the limitation "wherein the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature," however the relation defined by these claims is undefined. Recitation of the term "related" is so broad that the only interpretation excluded from this language would be "unrelated" or "not related". One reasonable interpretation of the claim would rely on the observation that all of power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature are inherently related to each other in the field of integrated circuits, as would be recognized by a person of ordinary skill in the art, and therefore the claim would be anticipated by a variable "related to an integrated circuit". Recognizing that integrated circuit model numbers commonly denote operating temperatures or required power

supply voltages, it is unclear what is properly excluded from the language of this claim. The language fails to particularly point out and distinctly claim the invention.

Regarding claims 4, 13, and 25, the independent claim 1 which is directed to a method, recites steps of "providing an equation", "replacing the unknown constants [...] to obtain a performance model", and "performing a first set of timing analyses using the performance model". While these steps are not indefinite per se, they broadly define an abstract method. For example, the claim contains no positive recitation of how to "provide an equation", what is literally involved in "obtaining a performance model", what type of timing analyses are performed, or how the timing analyses use the performance model. These recitations in claim 1 may not be improper under 35 U.S.C. § 112, however they create difficulties regarding claims 4, 13, and 25.

Dependent claims 4, 13, and 25 attempt to recite further limitations in the form of additional structure of the equation. These claims do not further limit the method of claim 1. Because claim 1 vaguely and broadly recites the use of the equation, the additional structure recited in claims 4, 13, and 25 have no direct relation to the method steps of claim 1. The inclusion of, for example "delay expressions" in the equation of claim 1 does nothing to limit the method defined by claim 1 because there exists no positive recitation in claim 1 of how the method depends upon, uses, manipulates, or recognizes "delay expressions" in the equation. Therefore, the method of claim 4 is functionally equivalent to the method of claim 1, and similarly claims 13 and 25.

The metes and bounds of claims 4, 13, and 25, as intended by claim language, are indefinite. It is unclear how these limitations further define the method of claim 1.

Dependent claims 5-12, 14-24, 26-35, and 40 stand rejected by virtue of their dependence and for the reasons stated above regarding claims 4, 13, and 25. The Examiner respectfully suggests that Applicants define a claimed method in terms of the steps performed rather than the structure of the components used in the method.

Claim 36 recites a limitation wherein "one of the variables is related to at least one of metallization capacitance and metallization resistance" however the relation defined by these claims is undefined. Claim 36 is rejected for the same reasons given above regarding claim 3.

Claims 38-39 recite limitations "wherein the plurality of variables are further related to metallization capacitance and metallization resistance" and "wherein the plurality of variables are further related to capacitive load" however the relation defined by these claims is undefined. Claims 38-39 are rejected for the same reasons given above regarding claim 3.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-6 and 7-35 and 37-40 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The numerous difficulties under 35 U.S.C. § 112, second paragraph, set forth above, necessitate this rejection of the claims under 35 U.S.C. § 112, first paragraph. The claims as drafted are drawn to an invention that is not disclosed in the specification. The method defined by the explicitly recited claim language of claims 1 and 37, as explained above, fails to require several critical steps. Specifically, the disclosed inventive method is not required by the method defined in these claims. Applicants are respectfully encouraged to draft claims that are limited to the disclosed invention.

Claim Interpretation

Because of the 35 U.S.C. § 112, first and second paragraph rejections, the claims are so indefinite and incomplete that no art rejection would be warranted, as substantial guesswork would be involved in determining the scope and content of these claims. It is essentially unknown what the metes and bounds of the claims are or where Applicants intend for those metes and bounds to lie. See *In re Steele,* 305 F.2d 859, 134 USPQ 292 (CCPA 1962); *Ex parte Brummer,* 12 USPQ 2d, page 1654; and also *In re Wilson,* 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). However, in the interest of compact prosecution, an art rejection will be asserted in view of the broadest and most reasonable interpretation of the claims. *Ex parte Ionescu,* 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

The claimed invention is interpreted as:

A method of making an integrated circuit, comprising:

Using a circuit simulator to simulate a first circuit design;

Calculating the effects of metallization capacitance and metallization resistance in the first circuit design using the circuit simulator;

Computing variables in an equation that models the performance of the first circuit design so that the variables correspond to the first circuit design;

Determining if the performance of the first circuit, modeled by the equation, meets predetermined criteria; and

Making an integrated circuit according to the first circuit design if the performance meets the predetermined criteria, else changing the first circuit design to obtain a second circuit design and repeating the steps of calculating, computing, and determining as applied to the second circuit design.

Claim 36 appears to recite an apparatus that performs the method of claim 1.

It is noted, however, that claims 1 and 37 merely require rejection of the following interpretations:

1. A method for making an integrated circuit, comprising:

Providing a first circuit design;

Changing the first circuit design to obtain a second circuit design; and

Making an integrated circuit comprising the second circuit design.

37. A method for obtaining a performance model, comprising:

Providing a path comprising a first design block, a second design block, and an interconnect coupling the first design block to the second design block;

Changing the design of at least one of the interconnect, the first design block, and the second design block to obtain a revised path; and

Making an integrated circuit comprising the revised path.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to

the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

4. Claims 1-6 and 9-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,018,623 to Chang et al. (Chang).

Chang teaches the influence of metallization resistance and metallization capacitance on integrated circuit performance and the importance of estimating (simulating) these effects during integrated circuit design [*"Variations in interconnect resistance ® and capacitance © create variances in the circuit delay and crosstalk. If the circuit delay or interconnect crosstalk for a chip exceeds the specification of the critical circuit path on the chip, a circuitry failure will occur. Therefore, it is important to accurately estimate the circuit delay variances for purpose of performance and yield tuning."* (column 1, lines 40-64)].

Chang teaches variables that are related to metallization resistance and metallization capacitance [*"As examples, the thickness, length and width of an interconnect will affect resistance, and the spacing between interconnects will affect capacitance."* (column 1, line 65 – column 2, line 7)].

Chang teaches using a circuit simulator to estimate the performance an integrated circuit based on the metallization resistance and metallization capacitance [*"In a final phase, the randomized RC nets are employed to determine worst-case values for one or both of delay and crosstalk. In the preferred embodiment, a device model is input, enabling estimation of delay*

and crosstalk for the entire circuit. The 3-sigma delay and crosstalk can be determined from a number of simulations, such as SPICE simulations or a fast delay calculator." (column 4, lines 26-52)].

Chang discloses numerous equations used to model the performance of the integrated circuit design [(column 6, line 65 – column 15, line 3)].

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to change a circuit design that fails to meet certain predetermined criteria, such as circuit timing and delay requirements. Teaching and motivation to do so would be found in the knowledge of a person of ordinary skill in the art of integrated circuit design.

Conclusion

The prior art made of record on form PTO-892 has not been relied upon and is considered pertinent to applicant's disclosure. Careful consideration of the cited art is required prior to responding this Office Action. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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